# DIGITAL VERIFICATION TOOLS

## 150 MHz Pulse Generator for Real-World Digital Signals

## HP 8110A

- VFO and PLL timing
- 10 ps resolution
- 2 ns variable transitions
- 20 V into 50 Ω
- Pulse, burst and data modes
- 3- and 4-level signals
- Configurable
- Master/slave capability


DESIGNED FOR HP-IB SYSTEMS

HP Instrument Drivers

HP 8110A + 2x HP 81103A

## HP 8110A Pulse Generator

Precise edge-positioning, plus the ability to simulate digital signals as they occur in the real world, make this pulse generator stand out as a partner for your HP oscilloscope or logic analyzer.

On the bench you can verify designs, achieving reliable results quickly at frequencies where emulation becomes uncertain or cumbersome.

In systems, high resolution lets you optimize yield. True-to-life signals improve measurement credibility.

The HP 8110A pulse generator can be factory-configured with one or two channels and can include a PLL module and a Deskew module. The second channel and the modules are retrofitable.

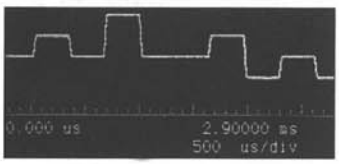
7

### Real-World Signals for Testing Digital Designs

Clock and data signals can be set up in the main channels, a separate strobe channel is available for device control signals. For more channels, two or more units can be master/slaved.


Through internal channel addition you can model high-frequency effects so that you can perform measurements before making substantial hardware investment. Many effects can be set up, such as irregular pulse widths, overshoot, pulse droop, ripple, crosstalk, reflections, ground-bounce, etc.


Three-/four-level waveforms are also solved using waveform addition. The picture here shows part of a 2B1Q communications signal generated by an HP 8110A.




### Bench Features

- All parameters at a glance, easy entry through knob or key pad, plus graphic visualization mean rapid error-free setups
- Setups internally storable, or on 95LX-type memory cards
- Timing conflicts quickly resolved with the autoset key or the intelligent help feature

### Device Interfacing Features

- Test bed delays compensated at the device
- Level display valid for all load resistances
- Voltage or current settings, amplitude or levels, can be preset
- Voltage or current device protection
- Parameter terms to suit the measurement, e.g., frequency/period; duration/phase/duty cycle

### Measurement Confidence

To ensure reliable measurements with good long-term repeatability, the high-resolution pulse edges are fast and clean with remarkably low jitter. The PLL module enhances frequency resolution, stability and accuracy.

The thorough specifications are valid over a wide temperature range. This avoids temperature-dependent recals and hence contributes to consistent performance.

### Flexible Triggering

The PLL module provides an additional triggering layer so that the pulses even in an externally-triggered sequence can be synchronized to the system clock. This capability allows, for example, programmable wait loops to be set up in order to optimize microprocessor performance. A different example of two-layer triggering, useful for repetitive measurements, is where a data or burst sequence needs to be repeated at intervals without recourse to an external trigger.

### CAT Features

- Low profile saves rack space
- Optional rear-panel connectors and rack mounting
- SCPI standard commands—less learning, protects software from obsolescence
- Wide operating-temperature range, no derating
- International electro-magnetic compliance standards
- PLL module synchronizes with system clock
- Display can be switched off to enhance bus speed
- Built-in diagnostics



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## HP 8110A Brief Specifications (50 Ω load, 0 to 55° C)

Please refer to Data Sheet 5091-4945 for details.

### HP 8110A Mainframe

**Frequency:** 1.00 Hz to 150 MHz
**Period:** 6.65 ns to 999 ms
**Resolution** (best case): 10 ps
**Accuracy:** 5% + 100 ps
**Jitter:** 0.03% + 25 ps, rms
**Modes:** Continuous/externally-triggered/externally-gated sequences of pulses, double pulses, bursts, and patterns. Also external width.
**Burst Length:** 2 to 65536 pulses or double-pulses
**Strobe Channel:** 2 to 4096 bits, freely programmable
**Format:** NRZ
**Level:** TTL/ECL selectable
**Source Resistance:** 50 Ω, typical

### HP 81106A PLL/Ext. Clock Module

**Frequency:** 1.000 mHz to 150.0 MHz
**Period:** 6.65 ns to 999.0 seconds
**Resolution** (best case): 10 ps
**Accuracy:** 0.1%
**Jitter:** 0.003% + 20 ps, rms
**Stability:** 50 ppm/year, typical
**Trigger Modes:** Int. clock, with int. or ext. reference, as period source or trigger for bursts and patterns; ext. clock for synchronizing to system clock or master/slave operation

### HP 81103A Channel Module

**Timing**
**Delay:** 0.00 ns to 998 ms } mutually
**Double-Pulse:** 6.65 ns to 998 ms } exclusive
**Accuracy:** 5% + 1 ns
**Width:** 3.30 ns to 998 ms
**Accuracy:** 5% + 250 ps
**Jitter:** 0.03% + 25 ps, rms
**Transitions** (10 to 90% amplitude): 2.00 ns to 200 ms
**Accuracy:** 10% + 200 ps
**Overshoot, Ringing:** 5% + 20 mV

**Output Parameters (into 50 Ω load)**

| | 50 Ω source | 1k Ω source |
|---|---|---|
| Amplitude, p-p: | 100 mv to 10.0 V | 200 mV to 20.0 V |
| High level: | –9.90 to + 10.0 V | –18.8 to + 19.0 V |
| Low level: | –10.0 to + 9.90 V | –19.0 to + 18.8 V |
| (also programmable as current ±4.00 to ±400 mA) | | |
| Limits: programmable to suit and protect device | | |

**Source Resistance:** 50 Ω/1 kΩ, selectable
**Load Resistance:** Values 0.1 Ω to 999 kΩ can be entered for direct-reading display of output level
**Modes:** Normal/complement, on/off

**Channel Addition (with two HP 81103A output channels):**
Simulates digital signals with interference pulses, or 3- or 4-level communications signals. Added waveform at Output 1. Output 2 disabled. 48/500 Ω source selectable.

**For Source Resistance 48 Ω Selected:** Amplitude: 0 to 19.5 Vp-p. Bipolar signals limit between 10 Vp-p (0.2 V/10.3 V peak levels) and 14 Vp-p (+7 V/–7 V peak levels).

**Minimum Transitions:**
Channel 1: 2.5 ns typ. (optimized for speed so that fast interference pulses can be added to "clean" channel 2 data)
Channel 2: 7.5 ns typ.

**For Source Resistance 500 Ω Selected:**
**Amplitude:** 0 to 20 Vp-p
**Minimum Transitions:** 30 ns typ. (both channels)

**Pattern Capabilities**
2 to 4096 bits. Edit capabilities include prbs $2^n$–1 where n is selectable from 7 to 12. Value 12 is CCITT O.151-compatible.
**Format:** RZ (width and delay programmable), DNRZ (delay programmable), NRZ

### HP 81107A Two-Channel Deskew Module

Compensates for unequal propagation times in the test setup, or for slave propagation delay in master/slave setups.
**Delay** (each channel): 0.00 to 28.00 ns plus typ. 6.5 ns

### General

**HP-IB Capability**
**Conformity:** IEEE 488.2, 1987, SCPI 1992.0
**Function Code:** SH1, AH1, T6, L4, SR1, RL1, PP0, DC1, DT1, C0

**Storage of Instrument Settings**
Current settings are retained on power-down. A default setting is implemented on RCL0 or HP-IB "*RST." Nine locations are available for user settings. Additionally, 40 settings can be stored on a 128 KB PCMCIA memory card (access time ≤300 ns), available as HP 8110A Option UFH. Note that a change in instrument configuration invalidates the files (save settings to disk via HP-IB before adding or removing HP 8110A modules.)

**Environmental**
**Temperature:** 0° to 55° C operating, –40° to 70° C storage
**Humidity:** 95% RH at 0° to 40° C
**Power:** 100 to 240 V ac ±10%, 50 to 60 Hz,
100 to 120 V ac ±10%, 50 to 60/400 to 440 Hz
**Consumption:** 300 VA (max. configuration)
**EMC Conformity:** CISPR 11, A; EN55011, A; EN50082-1
**Size:** 426 mm W x 89 mm H x 445 mm D (17 in x 3.3 in x 17.5 in)
**Weight:** Net 9.2 kg; shipping, 20.2 kg
**Recal Period:** 1 year recommended
**Warranty:** 3 years

| Ordering Information | Price |
|---|---|
| **HP 8110A** Mainframe (includes English operating and programming manual 08110-91012) | $5,650 |
| Always order at least one HP 81103A with each HP 8110A. A second HP 81103A or an HP 81106A or HP 81107A– in any combination–can be ordered at the same time or fitted retrospectively. | |
| **HP 81103A** Output Module | $4,750 |
| **HP 81106A** PLL/Ext. Clock Module | $1,550 |
| **HP 81107A** Deskew Module | $1,250 |
| **HP 8110A Options** | |
| **Opt 0B2** Additional Manual 08110-91012 | +$61 |
| A user guide of your choice can be obtained with each HP 8110A: | |
| **Opt ABD** German 08110-91112 | $0 |
| **Opt ABE** Spanish 08110-91412 | $0 |
| **Opt ABF** French 08110-91212 | $0 |
| **Opt AB1** Korean 08110-91812 | $0 |
| **Opt ABJ** Japanese 08110-91512 | $0 |
| **Opt ABZ** Italian 08110-91312 | $0 |
| For further user guide requirements, please order the part number quoted above, not the option number. Use the English OPM 08110-91012 for programming. | |
| **Opt UFH** 128 kB Memory Card | +$160 |
| **Opt UN2** Rear- (instead of front-) panel Connectors | $0 |
| **Opt 1CN** Front-handle Kit (5062-3988) | +$56 |
| **Opt 1CP** Rack-mount/Handle Kit (5062-3975) | +$82 |
| **Opt 1CM** Rack-mount Kit (5062-3974) | +$36 |
| **Opt 1CR** Rack-slide Kit (1494-0060) | +$122 |
| **Opt 1BP** MIL-45662A Cal with Test Data | +$715 |
| **Opt 0BW** Service Manual (08110-91021) | +$102 |
| **Opt 503** Front- and Rear-panel Connectors | Contact factory |
| **HP 08110-91031** Component-level Service Documentation | $100 |





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